L2106S

高电压半桥驱动芯片

1. 功能说明

L2106S是高电压、快速的 MOSFET 及 IGBT 半桥驱动芯片。芯片的逻辑输入端与标准 CMOS 及 TTL 输出讯号兼容，并具有防止上桥及下桥同时输出造成的导通短路保护(short-through prevention) 以及 UVLO 电路防止 VCC 低于导通开启电压造成的误动作。

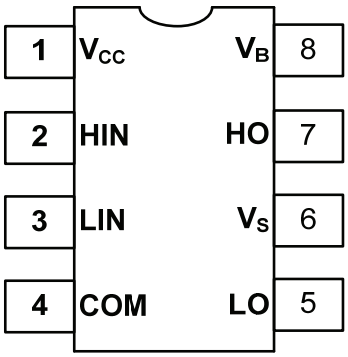
2. 芯片特色

- 上桥的浮动信道电压设计可用于 600V 的 bootstrap 电路操作
- UVLO 功能
- 输出的闸极电压可达 10 到 20 V
- 5V 及 15V 的逻辑输入
- 防止上桥及下桥同时输出造成的导通短路保护
- 内部停滞时间(dead-time)控制
- 上下通道具有兼容的传递延迟
- 输出与输入讯号同步
- 符合 RoHS

3. 应用领域

- 直流马达、电动车、镇流器及音响放大器

4. 引脚外观



8 Lead SOIC

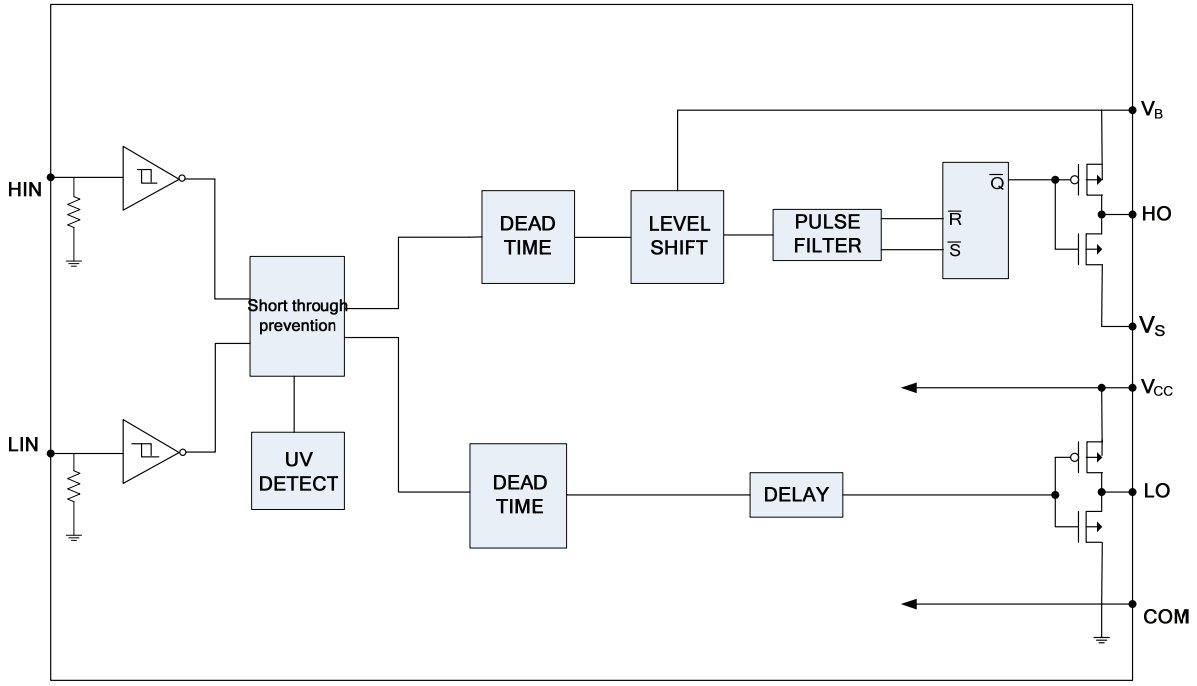
5. 外观打印方式

Product Name	Marking
L2106S	L2106S XXXXX X : Date Code

6. 引脚定义

脚位	名称	说明
1	V_{CC}	下桥及逻辑电源
2	HIN	上桥闸级输出的上桥逻辑输入讯号引脚
3	LIN	下桥闸级输出的下桥逻辑输入讯号引脚
4	COM	接地
5	LO	下桥闸级输出讯号引脚
6	V_S	上桥浮动电源接上桥 MOSFET 源极引脚
7	HO	上桥闸级输出讯号引脚
8	V_B	上桥浮动电源引脚

7. 电路方块图



8. 绝对操作范围

Absolute maximum ratings indicate sustained limits and beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	600	V
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	- 0.3	20	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	- 0.3	V_{CC} + 0.3	
dV_S / dt	Allowable offset supply voltage transient	-	50	V / ns
P_D	Package power dissipation @ $T_A \leq +25^oC$ (8 lead SOIC)	-	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient (8 lead SOIC)	-	200	ºC / W
T_J	Junction temperature	-	150	ºC
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

9. 建议操作范围

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	- 2	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	- 40	125	ºC

10. 标准静态电气特性数值

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, T_A = 25 ºC unless otherwise specified. The V_{IN}, $V_{TH\ and}$ I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads : HO or LO.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic " 1 " input voltage	V_{CC} = 10 V to 20 V	4	-	-	V
V_{IL}	Logic " 0 " input voltage	V_{CC} = 10 V to 20 V	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	-	-	100	mV
V_{OL}	Low level output voltage		-	-	100	
I_{LK}	Offset supply leakage current	V_B = V_S = 500 V	-	-	60	uA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	-	25	-	
I_{QCC}	Quiescent V_{CC} supply current	V_{IN} = 0 V or 5 V	-	300	-	
I_{IN+}	Logic " 1 " input bias current	V_{IN} = 5 V	-	5	15	
I_{IN-}	Logic " 0 " input bias current	V_{IN} = 0 V	-	-	15	
V_{CCUV+}	V_{CC} supply under voltage positive going threshold		7.8	8.8	9.8	V
V_{CCUV-}	V_{CC} supply under voltage negative going threshold		7	8.0	9.0	
I_{O+}	Souring current		-	250	-	mA
I_{O-}	Sink current		-	320	-	mA

11. 标准动态电气特性数值

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 ºC, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	-	1000	-	ns	VS = 0 V
t_{off}	Turn-off propagation delay	-	500	-		VS = 0 V or 600 V
t_r	Turn-on rise time	-	100	-		
t_f	Turn-off fall time	-	50	-		VS = 0 V
MT	Delay matching $\lvert t_{on} - t_{off} \rvert$	-	-	50		
DT	Dead-time : LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	-	560	-		

Note：PWM pulse width should be ≧ 1 μsec.

12. 时序图

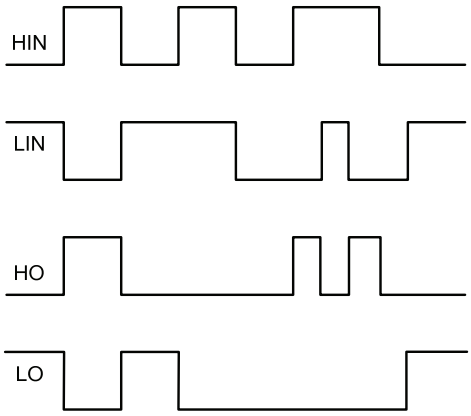


Figure 1. Input / Output Timing Diagram

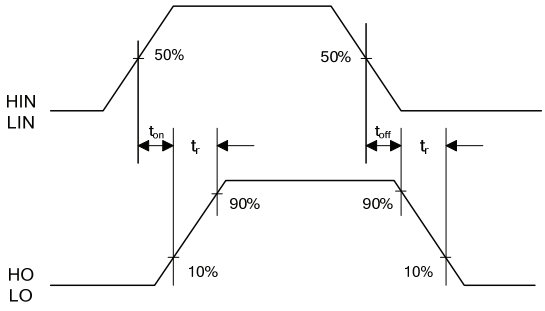


Figure 2. Switching Time Waveform Definitions

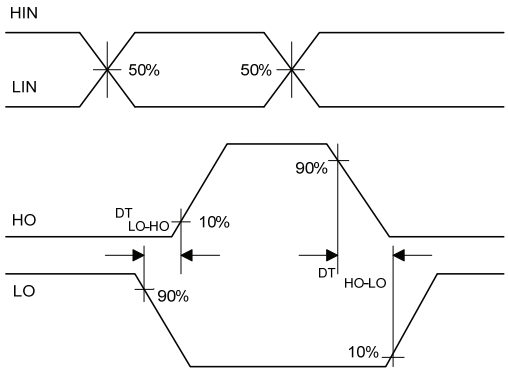
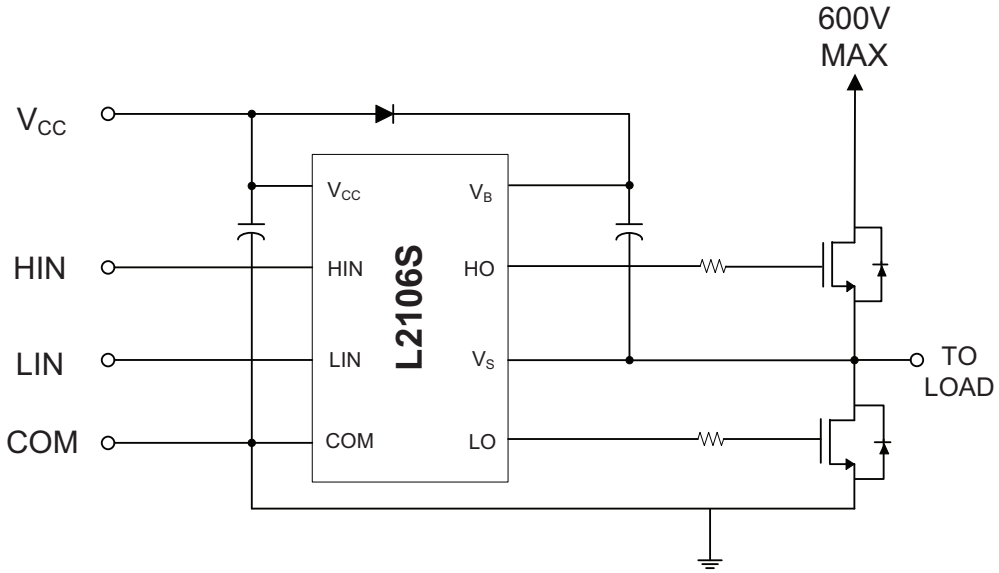


Figure 3. Dead-time Waveform Definitions

13. 应用电路



14. 标准电气特性图形

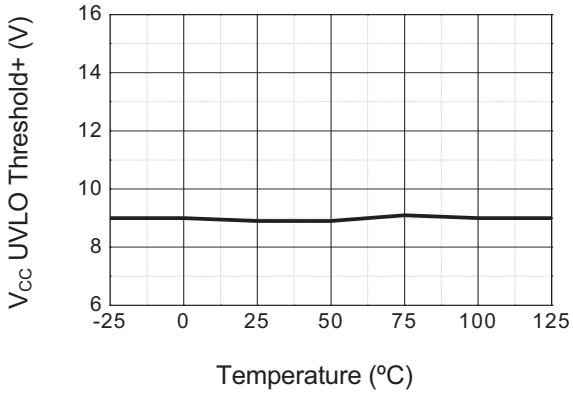


Figure 1. Vcc UVLO Threshold+ vs Temperature

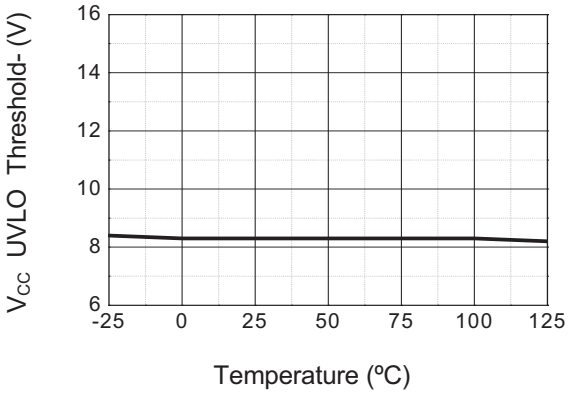


Figure 2. Vcc UVLO Threshold- vs Temperature

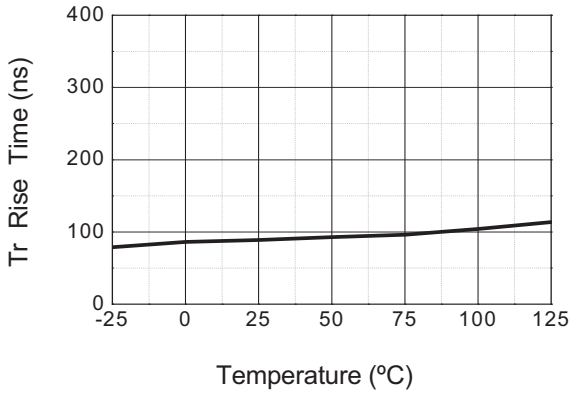


Figure 3. Tr Rise Time vs Temperature

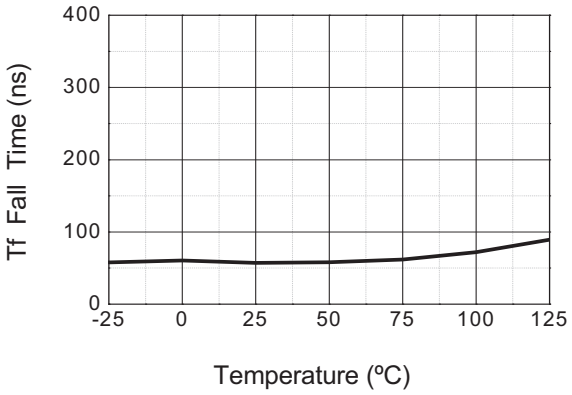


Figure 4. Tf Fall Time vs Temperature

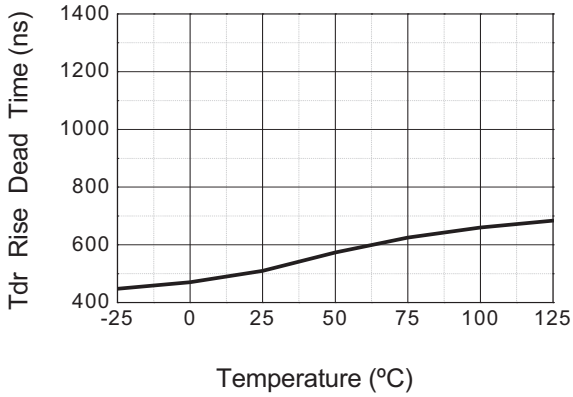


Figure 5. Tdr Rise Dead Time vs Temperature

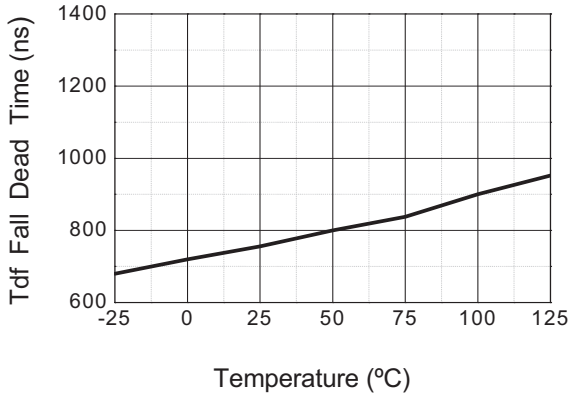


Figure 6. Tdf Fall Dead Time vs Temperature

14. 标准电气特性图形(续)

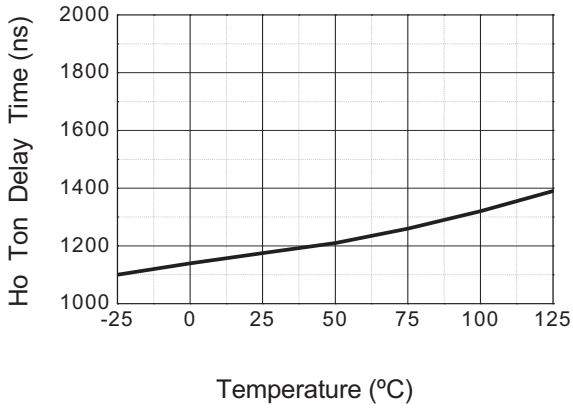


Figure 7. Ho Ton Delay Time vs Temperature

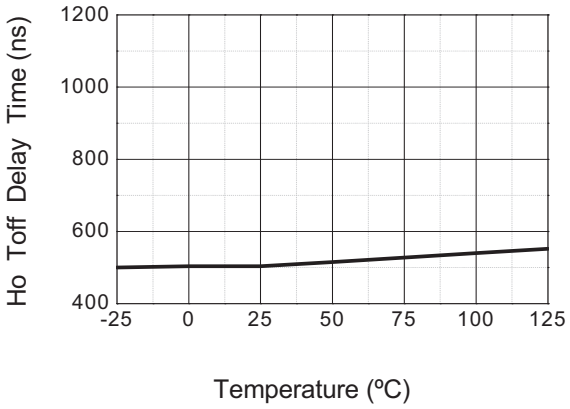


Figure 8. Ho Toff Delay Time vs Temperature

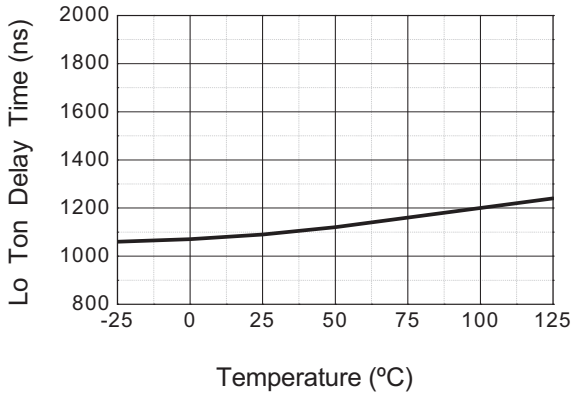


Figure 9. Lo Ton Delay Time vs Temperature

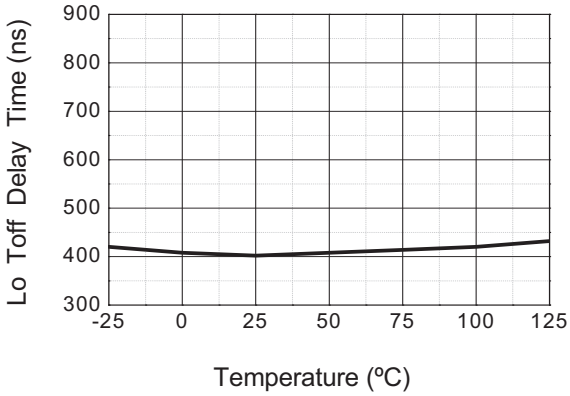


Figure 10. Lo Toff Delay Time vs Temperature

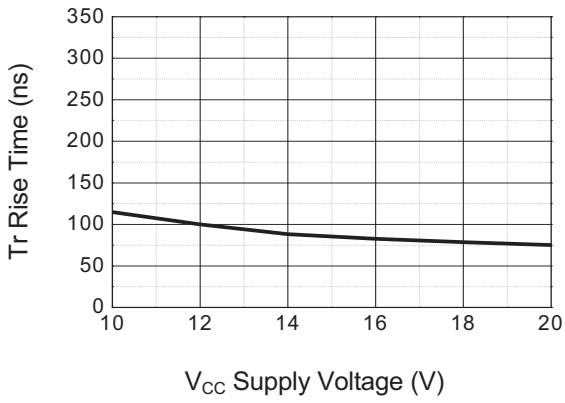


Figure 11. Tr Rise Time vs V_{CC} Supply Voltage

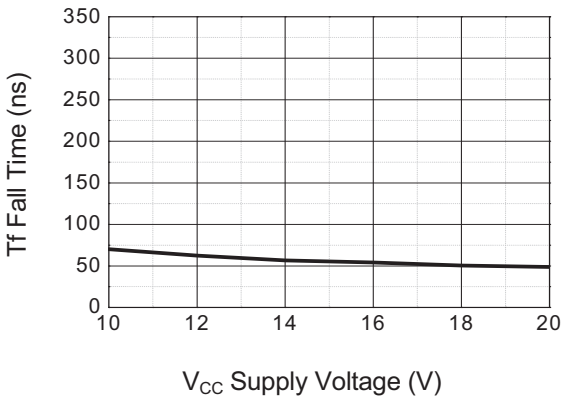


Figure12.Tf Fall Time vs V_{CC} Supply Voltage

14. 标准电气特性图形(续)

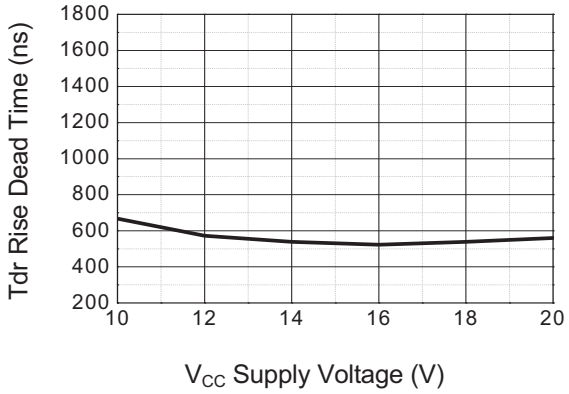


Figure 13. Tdr Rise Dead Time vs Vcc Supply Voltage

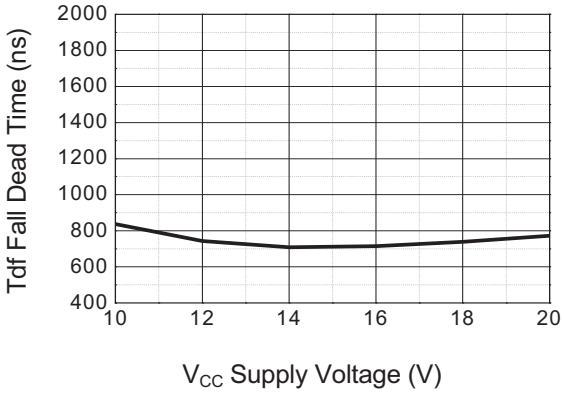


Figure 14. Tdf Fall Dead Time vs Vcc Supply Voltage

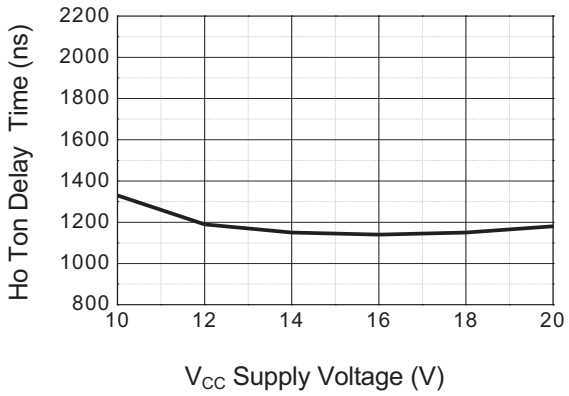


Figure 15. Ho Ton Delay Time vs V_{CC} Supply Voltage

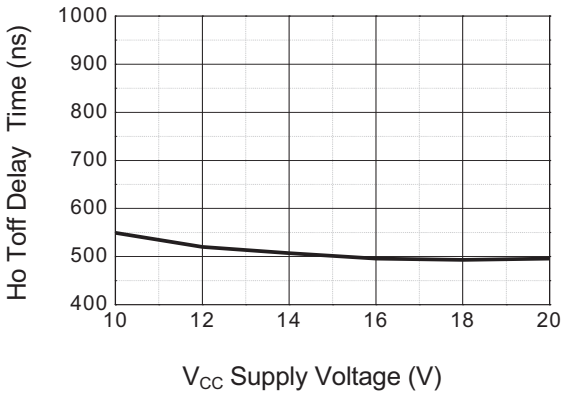


Figure 16. Ho Toff Delay Time vs V_{CC} Supply Voltage

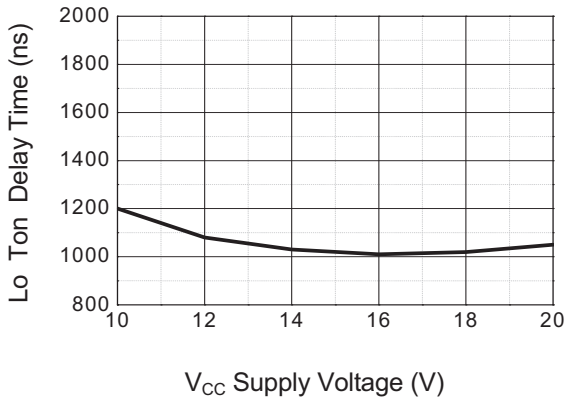


Figure 17. Lo Ton Delay Time vs V_{CC} Supply Voltage

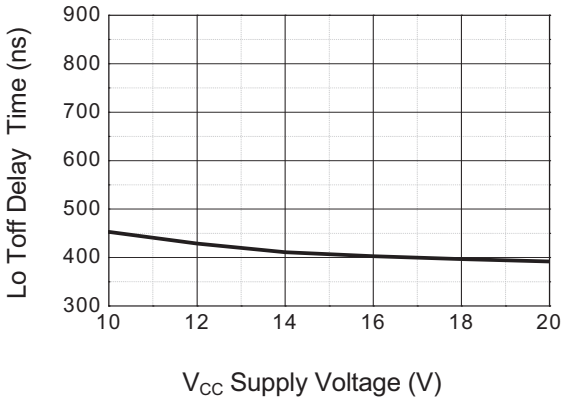
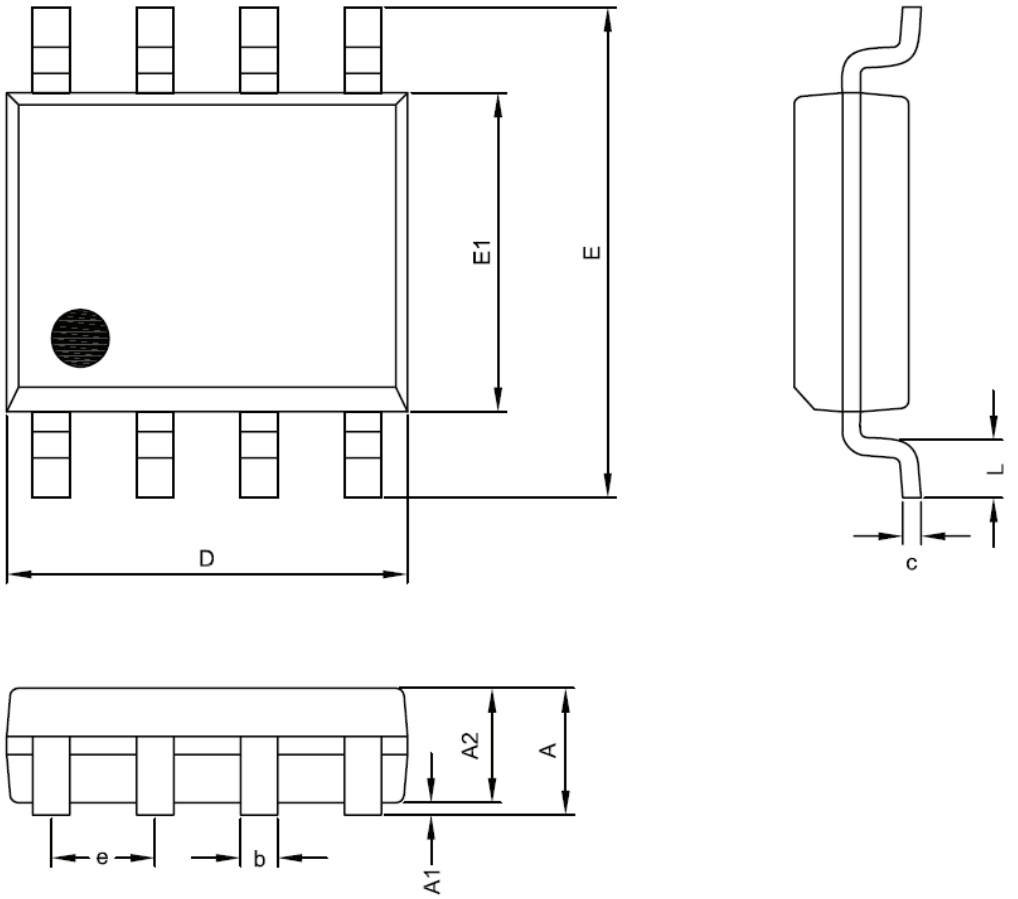


Figure18. Lo Toff Delay Time vs V_{CC} Supply Voltage

15. 封装信息

SOP- 8



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.