L2001S

High Side and Low Side Driver

1. 功能说明

L2001S 是高电压、快速的 MOSFET 半桥驱动芯片。芯片的逻辑输入端与标准 CMOS 及 TTL 输出讯号兼容，并具有防止上桥及下桥同时输出造成的导通短路保护(short-through prevention) 以及 UVLO 电路防止 VCC 低于导通开启电压造成的误动作。
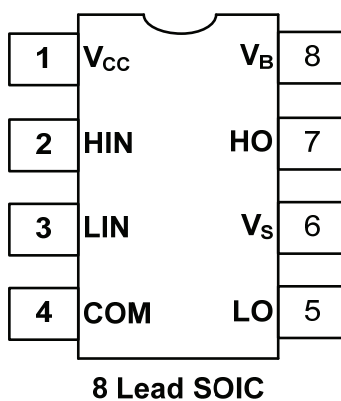
2. 芯片特色

- 上桥的浮动信道电压设计可用于 200V 的 bootstrap 电路操作
- UVLO 功能
- 输出的闸极电压可达 10 到 20 V
- 5V 及 15V 的逻辑输入
- 防止上桥及下桥同时输出造成的导通短路保护
- 内部停滞时间(dead-time)控制
- 上下通道具有兼容的传递延迟
- 输出与输入讯号同步
- 符合 RoHS

3. 应用领域

- 直流马达、电动车、镇流器及音响放大器

4. 引脚外观

1	V_CC	V_B	8
2	HIN	HO	7
3	LIN	V_S	6
4	COM	LO	5

8 Lead SOIC

5. 外观打印方式

| Product Name	Marking
L2001S	L2001S XXXXX X : Date Code

6. 订购信息编码

L2001S └── Assembly Material	Assembly Material G: Halogen and Lead Free Device

Note: LUL defines " Green " as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

7. 引脚定义

脚位	名称	说明
1	V_{CC}	下桥及逻辑电源
2	HIN	上桥闸级输出的上桥逻辑输入讯号引脚
3	LIN	下桥闸级输出的下桥逻辑输入讯号引脚
4	COM	接地
5	LO	下桥闸级输出讯号引脚
6	V_S	上桥浮动电源接上桥 MOSFET 源极引脚
7	HO	上桥闸级输出讯号引脚
8	V_B	上桥浮动电源引脚

8. 电路方块图
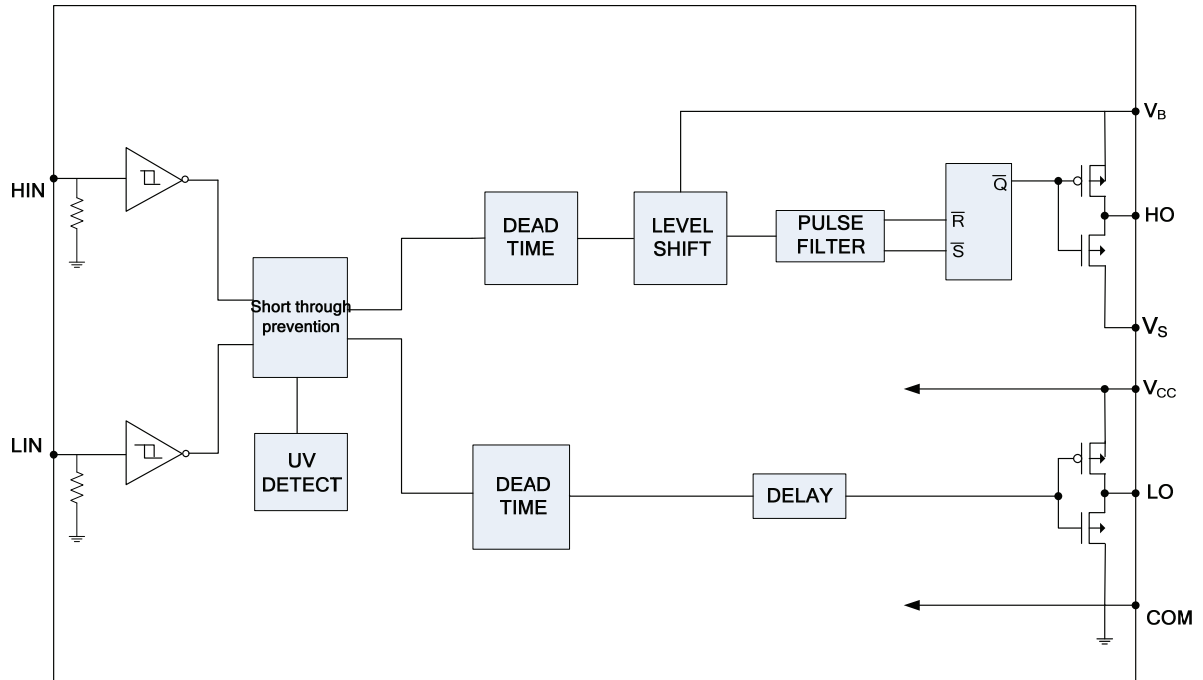
9. 绝对操作范围

Absolute maximum ratings indicate sustained limits and beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	- 0.3	200	V
V_S	High side floating supply offset voltage	V_B - 20	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	- 0.3	20	
V_{LO}	Low side output voltage	- 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	- 0.3	V_{CC} + 0.3	
dV_S / dt	Allowable offset supply voltage transient	-	50	V / ns
P_D	Package power dissipation @ $T_A \le$ + 25 $^\circ$C (8 lead SOIC)	-	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient (8 lead SOIC)	-	200	$^\circ$C / W
T_J	Junction temperature	-	150	$^\circ$C
T_S	Storage temperature	- 55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

10. 建议操作范围

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	- 2	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	- 40	125	$^\circ$C

11. 标准静态电气特性数值

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, T_A = 25 ºC unless otherwise specified. The V_{IN}, $V_{TH \, and}$ I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads : HO or LO.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic " 1 " input voltage	V_{CC} = 10 V to 20 V	4	-	-	V
V_{IL}	Logic " 0 " input voltage	V_{CC} = 10 V to 20 V	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	-	-	100	mV
V_{OL}	Low level output voltage		-	-	100	
I_{LK}	Offset supply leakage current	V_B = V_S = 200 V	-	-	60	uA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	-	25	-	
I_{QCC}	Quiescent V_{CC} supply current	V_{IN} = 0 V or 5 V	-	300	-	
$I_{IN +}$	Logic " 1 " input bias current	V_{IN} = 5 V	-	5	15	
$I_{IN -}$	Logic " 0 " input bias current	V_{IN} = 0 V	-	-	15	
$V_{CCUV +}$	V_{CC} supply under voltage positive going threshold		7.8	8.8	9.8	V
$V_{CCUV -}$	V_{CC} supply under voltage negative going threshold		7	8.0	9.0	
$I_{O +}$	Souring current		-	250	-	mA
$I_{O -}$	Sink current		-	320	-	mA

12. 标准动态电气特性数值

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 ₚF, T_A = 25 ºC, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	-	1000	-	ns	VS = 0 V
t_{off}	Turn-off propagation delay	-	500	-		VS = 0 V or 200 V
t_r	Turn-on rise time	-	100	-		
t_f	Turn-off fall time	-	50	-		VS = 0 V
MT	Delay matching $\mid t_{on} - t_{off} \mid$	-	-	50		
DT	Dead-time : LO turn-off to HO turn-on ($DT_{LO - HO}$) & HO turn-off to LO turn-on ($DT_{HO - LO}$)	-	560	-		

Note：PWM pulse width should be $\geqq$ 1 μsec.
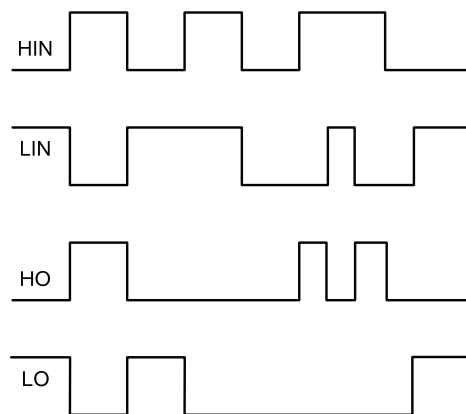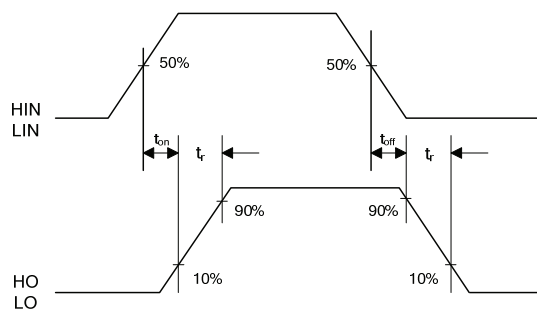
13. 时序图

Figure 1. Input / Output Timing Diagram
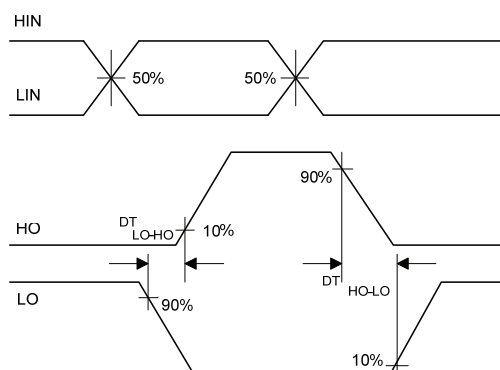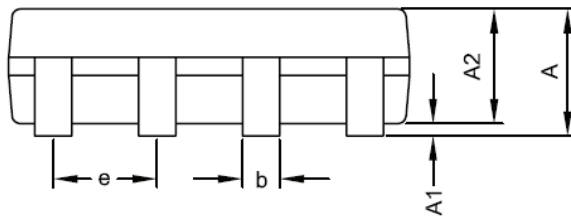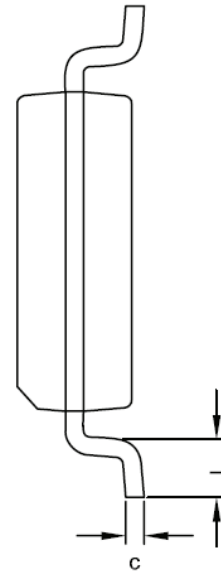

Figure 2. Switching Time Waveform Definitions

Figure 3. Dead-time Waveform Definitions

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14. 应用电路

![LUL logo]

L2001S
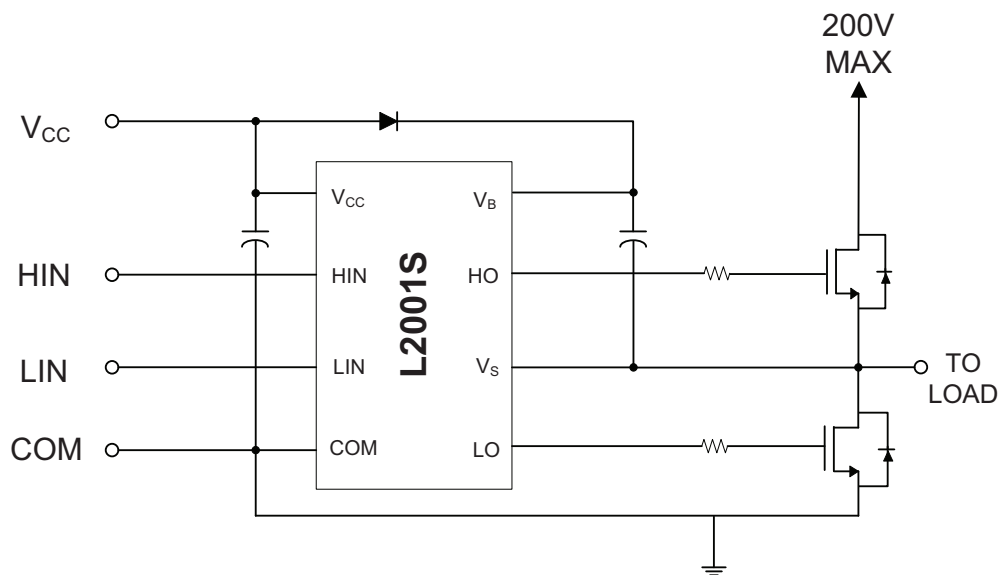
15. 封装信息

SOP- 8
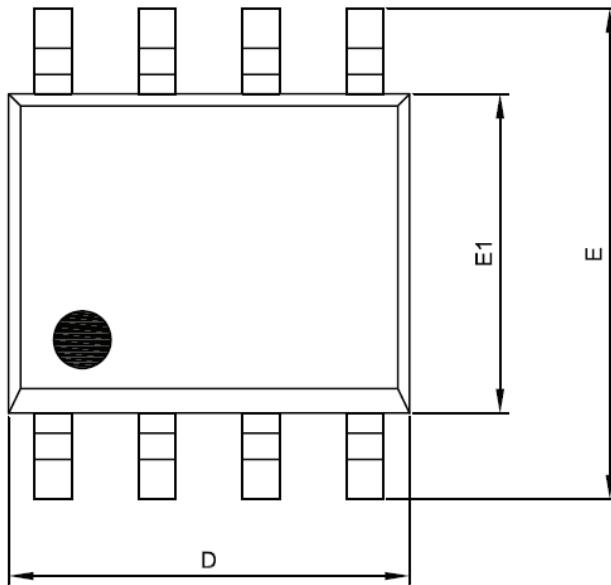
Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：
1. Jedec outline ： MS-012AA
2. Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .
3. Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.